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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,497	10/26/2001	Er-Xuan Ping	MTI-31041-A	8624

22202 7590 03/10/2006

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/046,497	PING ET AL.
	Examiner	Art Unit
	Thao X. Le	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2005*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *101-116 and 123-224* is/are pending in the application.

4a) Of the above claim(s) *101-116,123-142,156-166,194 and 195* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *143-155,167-193 and 196-226* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 14 Feb. 2006 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 225-226 are rejected under 35 U.S.C. 102(b) as being anticipated by JP401286361 to Matsumoto.

Regarding claim 225 and 226, Matsumoto discloses a raised structure in fig. 3 on a substrate 1 comprising a plurality of overlying layers 4/6 of epitaxial silicon, each of said silicon layer 4/6 having an upper surface comprising a plurality of facets, and sidewalls with an insulative layer 3 thereover, and wherein an uppermost silicon layer 6 comprises a conductivity enhancing dopant, see attached abstract and constitution.

4. Claims 143-144, 147, 149-153, 167, 169-170, 172-173, 175-176, 178-179, 181-193, and 196-223 are rejected under 35 U.S.C. 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over JP401286361 to Matsumoto.

Regarding claims 143, 182, 186, 197, 201, Matsumoto discloses a semiconductor structure in fig. 3, comprising at least two overlying faceted layers 4/6 of single crystal epitaxial silicon (ES), each ES layer comprising a faceted surface comprising a plurality of facets, fig. 3, and sidewalls with insulative materials 3 thereover, and an uppermost faceted layer of at least two overlying layers of ES having a layer of an insulative material 5 over the faceted surface of uppermost layer of ES, wherein the structure is situated on a substrate 1 in a vertical orientation, fig. 3 and attached abstract and constitution.

With respect to the 'single crystal", Matsumoto uses the SEG (selective epitaxial growth) that is a process that deposit single crystal silicon layers only on the exposed silicon substrate surface within the opening in the dielectric mask. Such definition can be found in Lee (US6228733) in col. 1 lines 20-25. When the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding to claims 144, 147, Matsumoto discloses the semiconductor structure wherein the insulative crystal 5 comprises an oxide.

Regarding to claims 149, 190, 196, 198, 202, Matsumoto discloses a semiconductor structure in fig. 3, comprising at least two overlying faceted layers 4/6 of single crystal ES, each of said layers comprising a faceted surface comprising a plurality of facets, sidewalls, and an insulative materials 3 over the sidewalls, an uppermost layer of the at least two overlying layers 33/34 having a layer of an insulative material 41 over the top faceted surface, one or more of the layers of ES comprising a conductivity enhancing dopant, see attached abstract and constitution, wherein the structure is situated on a substrate in a vertical orientation.

With respect to the 'single crystal", Matsumoto uses the SEG (selective epitaxial growth) that is a process that deposit single crystal silicon layers only on the exposed silicon substrate surface within the opening in the dielectric mask. Such definition can be found in Lee (US6228733) in col. 1 lines 20-25. When the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claims 150-153, Matsumoto discloses the conductivity enhancing dopant comprising a p-type dopant, which is selected from the group consisting of

boron, wherein the conductivity enhancing dopant comprising a n-type dopant, which is selected from the group consisting of phosphine, see attached abstract and constitution.

Regarding claims 167, 169-170, 172, 175-176, 178-179, 181, 183-185, 187-189, 191-193 Matsumoto discloses the semiconductor structure being a component of a transistor, and being a S/D diffusion region, fig. 1-3.

Regarding to claims 173, 176, 199, Matsumoto discloses a semiconductor structure in fig. 3, comprising at least two overlying faceted layers 4/6 of single crystal epitaxial silicon (ES) including an uppermost faceted layers of single crystal ES 6; each of said faceted layers comprising a faceted top surface comprising a plurality of facets, and insulated sidewalls, and the uppermost faceted layer of ES having an insulated top surface; the structure is situated on a substrate in a vertical orientation, wherein the structure being a component of a transistor, fig. 1-3.

With respect to the 'single crystal", Matsumoto uses the SEG (selective epitaxial growth) that is a process that deposit single crystal silicon layers only on the exposed silicon substrate surface within the opening in the dielectric mask. Such definition can be found in Lee (US6228733) in col. 1 lines 20-25. When the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding to claims 179, 200, Matsumoto discloses a semiconductor structure in fig. 3, comprising at least two overlying faceted layers of single crystal ES 4/6, each said faceted layers comprising a faceted top surface comprising a plurality of facets, sidewalls, and insulative materials 3 over the sidewalls, an uppermost faceted layer 6 of ES of the at least two overlying faceted layers 4/6 having a layer of an insulative material 5 over the top surface, one or more of at least two overlying faceted layers of ES comprising a conductivity enhancing dopant wherein the structure is situated on a substrate in a vertical orientation, and the structure being a component of a transistor, fig. 1-3.

With respect to the 'single crystal", Matsumoto uses the SEG (selective epitaxial growth) that is a process that deposit single crystal silicon layers only on the exposed silicon substrate surface within the opening in the dielectric mask. Such definition can be found in Lee (US6228733) in col. 1 lines 20-25. When the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claims 203-223, as discussed in the above claims 143, 149,173, 176, 179, 182, 186, 190, 196, 197-202, Matsumoto discloses the all the claimed structure limitations in claims 203-223. Claims 203-223 are product-by-process, thus all the

process limitations in claims 203-223 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 145-146, 148, 154-155, 168, 171, 174, 177, and 180 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP401286361 to Matsumoto in view of US 5483094 to Sharma et al.

Regarding claims 145-146 and 148, Matsumoto does not expressly disclose the thickness of the insulative layer comprises silicon nitride having thickness about 5 to 20 nm or 2 to 5 nm.

However, Sharma reference discloses an insulative layer 41/61 comprises silicon oxide and/or silicon nitride, col. 5 line 29-32, has a general thickness in fig. 12. Accordingly, it would have been obvious to one of ordinary skill in art to use the silicon nitride teaching Sharma in Matsumoto device in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955), and also because such material substitution would have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06.

Regarding claims 154-155, Matsumoto does not disclose the semiconductor structure wherein one or more of the layers of the ES comprises a concentration gradient of the dopant within the ES crystal, wherein the concentration gradient comprises a low to high concentration of the dopant within the ES, with the high dopant concentration at the top surface of the one or more of the layers.

However, Sharma discloses the semiconductor structure wherein one or more of the layers of the ES comprises a concentration gradient of the dopant within the ES crystal, wherein the concentration gradient comprises a low to high concentration of the dopant within the ES, with the high dopant concentration at the top surface of the one or more of the layers, column 3 line 55-67. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use grading doping teaching of Sharma with Matsumoto's device, because

it would have created a hot electron injection as taught by Sharma in col. 3 lines 66-67.

Regarding claims 168, 171, 174, 177, and 180, Matsumoto does not disclose the semiconductor structure being a transistor gate.

A recitation of 'being a transistor gate' of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07.

7. Claim 224 is rejected under 35 U.S.C. 103(a) as being unpatentable over JP401286361 to Matsumoto in view of US 5849077 to Kenney.

Regarding claim 224, Sharma does not disclose the semiconductor structure wherein the top surface of at lest one of epitaxial silicon crystal defines a face having a (100) plane orientation.

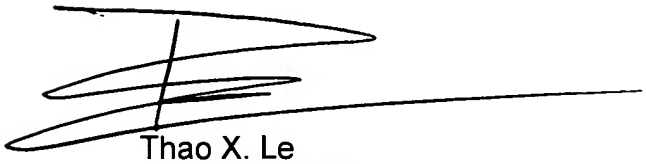
However, Kenney discloses a semiconductor structure in fig. 1m wherein the top surface of at lest one of epitaxial silicon crystal 19 defines a facet having a (100) plane orientation, column 4 line 39. The silicon substrate 1 is having a (100) plane orientation, column 4 line 11; thus the epitaxial layer 19 is having the same orientation. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the (100) plane orientation 19 teaching of Kenney in Sharma's device, because the (100) plane orientation is greatly dominated the market as taught by Kenney, column 2 lines 28-30.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao X. Le
01 March 2006